REMARKS

Claims 1-3 and 10 have been rejected under 35 U.S.C. 102(e) as being anticipated by Sung et al. (U.S. Patent No. 6,504,206).

Claims 1 and 3 have been canceled. Claim 4 (which is discussed below) has been amended to incorporate the limitations of base Claims 1 and 3. Claims 2 and 10 have been amended to depend from amended Claim 4 (and are therefore allowable for at least the same reasons as amended Claim 4, as described below).

Claim 9 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. and Yang et al. (U.S. Patent No. 5,973,353).

Claim 9 has been amended to depend from amended Claim 4 (and is therefore allowable for at least the same reasons as amended Claim 4, as described below).

Claims 4-6 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. and Pham et al. (U.S. Patent No. 6,242,306).

As described above, Claim 4 has been amended to incorporate the language of base Claims 1 and 3. Claim 4 recites "a first oxide region located over the first diffusion bit line; and a second oxide region located over the second diffusion bit line".

The Examiner correctly notes that Sung et al. fail to teach the first and second oxide regions/layers located over the diffusion bit lines BL-1 and BL-2.

The Examiner indicates that it would be obvious to put the first and second oxide regions/layers 19 located over bit lines 21-23 [sic] of Pham et al. in the device of Sung et al. to make an improved EEPROM.

However, if bit line oxide regions similar to those taught by Pham et al. were grown over source/drain regions 14 of Sung et al., a significant problem would exist. Sung et al. clearly teach that polysilicon sidewalls 15 (which are used to store charge) are formed by anisotropically etching a coating of polysilicon 14. (Sung et al. Col. 3, lines 27-31; Fig. 1d.) It is well established that sidewalls formed in this manner are typically very narrow (i.e., significantly narrower than the minimum line width of the process being used). Thus, bit line oxide regions grown over source/drain regions 14 would likely extend entirely under polysilicon sidewalls 15. (See, e.g., Applicant's specification at Fig. 10, which shows bit line oxide regions 442-444 extending under the edges of floating gate elements 404_{11}-404_{12}, 404_{21}-404_{22}, and 404_{31}-404_{32}.) In this case, polysilicon sidewalls 15 would be electrically isolated from source/drain regions 14 and substrate 10, such that these polysilicon sidewalls 15 would no longer operate as floating gate elements.

In addition, during the growth of the bit line oxide regions, the polysilicon sidewalls 15 would also be exposed to oxidizing conditions, thereby reducing the ability of these sidewalls to store charge.

For the above reasons, it is likely that forming the bit line oxide regions of Pham et al. with the structure of Sung et al. would result in non-operational cell.

Furthermore, although Pham et al. do not specify when the bit line regions 14 are formed (Pham et al., Col. 4, lines 15-20) it seems that these bit line regions 14 would have to be formed before the bit line oxide regions 19 (and therefore before the floating gate elements 24). (See, Pham et al., Figs. 3-8.) As a result, these bit line regions

cannot be self-aligned with the subsequently formed floating gate elements 24. This is inconsistent with Sung et al., which requires that the bit line regions 14 are aligned with polysilicon sidewalls 15. (See, Sung et al., Fig. 1d.)

Because of this inconsistency in the processes of Pham and Sung et al., it would not be obvious to combine the bit line oxide regions of Pham with the structure of Sung et al.

For these reasons, Claim 4 is allowable over Sung et al. in view of Pham et al. Claims 2 and 5-10, which depend from Claim 4, are allowable over Sung et al. in view of Pham et al. for at least the same reasons as Claim 4.

Claims 18-28 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. (U.S. Patent No. 6,281,545 in view of Pham et al.

The Examiner states "While the Examiner agrees that some of the processes of each of these prior art maybe inconsistent it does not necessarily mean that the features of these device could be combine in another way which is consistent with the inventive features expressed by both". However, as described below (and in the previous Office Action Response), the combination suggested by the Examiner is not consistent with the inventive features expressed by Liang et al. and Pham et al.

In rejecting Applicant's previous arguments, the Examiner states "In this case, the sidewalls of Liang et al. are not an essential feature of the invention (See, Column 1, lines 30 to 42 for the inventive structure). These sidewalls could be incorporated at the step shown in Figure 8 of Pham et al."

The Examiner's argument is not clear. If the sidewalls of Liang et al. are ignored (as they "are not an essential feature of the invention"), then both Liang et al. and Pham

et al. fail to teach or suggest "a first sidewall oxide region, having a different composition than the dielectric layer" and "a second sidewall oxide region, having a different composition than the dielectric layer", as recited by Claim 18.

Moreover, there is no motivation to combine a non-essential feature of Liang et al. (i.e., sidewalls 28) with Pham et al., as suggested by the Examiner, because Pham et al., already describes a dielectric layer located over the sidewalls of floating gate elements 24 (Pham et al., Fig. 10, barrier layer 17.) Thus, providing sidewalls "at the step shown at Fig. 8 of Pham et al." as suggested by the Examiner would simply add additional unnecessary steps to the process of Pham et al., without adding any additional features.

In addition, the Examiner's original argument indicated that the certain features of Pham et al. (i.e., "control gate over the first and second sidewall oxide regions, the first and second source/drain regions continuous with the first and second bit lines and first and second oxide regions/layers located over said bit lines") could be added to the structure of Liang et al. in order to render Claims 18-28 unpatentable. Conversely, the Examiner's current argument indicates that certain features of Liang et al. (i.e., "sidewalls") could be added to the structure of Pham et al. in order to render Claims 18-28 unpatentable. Because the Examiner's present argument is different than the argument appearing in the previous Office Action (and the Applicant did not amend Claims 18-28 in the previous Office Action), the finality of the present Office Action should be withdrawn.

For the above-stated reasons, Claim 18 is allowable over Liang et al. in view of Pham et al. Claims 19-28, which depend from Claim 18, are allowable over Liang et al. in view of Pham et al. for at least the same reasons as Claim 18.

CONCLUSION

Claims 2, 4-10 and 18-28 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION (37 C.F.R. 1.8(a))

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Date: Nov. 10, 2003 Signature: Carrie Peddick